Minimum Reactive Power Filter Design for High Power Converters.

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***Abstract*— This work proposes and evaluates an optimized filter design for high power converter with sinusoidal voltage and current. The inherent low switching frequency of this class of converters complicates the filter design and generally results in large filter components. The proposed design culminates in minimum filter reactive power, size and cost. Simulation and experimental results support those ideas.**

***Keywords*— High Voltage power converters, Passive filter, Harmonics, Power factor correction.**

I. INTRODUCTION

Many harmonic related issues have been reported recently [1] and [2]. They include excessive heating and losses in electrical machines and other electromagnetic equipments, winding over voltages, reduction of device life service and other problems. Regarding the utility grid, harmonics deteriorate the supplied voltage waveform and increase the electromagnetic emissions. On the other hand, sinusoidal voltage and current in an electrical system is highly desirable. Nevertheless, electronic apparatuses distort the grid current and voltage.

In many works, passive sinusoidal filters come out as good alternative to reduce the system harmonic content. The inherently low switching frequency of high power converters, limited from about 500 to 1000 Hz, complicates filter design, which generally results in large filter elements. Besides, due to grid resonance problems and poor filter attenuation the lower the switching frequency the more complex the filter design and worse filter performance are. Unfortunately in literature [2]-[8] only a small number of papers is devoted to multilevel structures ([2], [6] and [7]) and a number even smaller discusses the problem of filter design under very low switching frequency conditions. Still in this case design criteria result again in bulky filter components.

This paper proposes an enhanced passive filter configuration for high power converters. A complete filter design based on the optimization of the filter reactive power leads minimum cost weight and size. Besides, reasonably simple design steps culminate in unique and well-defined filter element values. The modulation strategy adopted in this paper is the Selective Harmonic Elimination-SHEPWM, which also results in simplifications on the filter design rules. Moreover, the modulator SHEPWM works under a classical voltage oriented synchronous reference frame control for a high power active rectifier. Simulation and experimental results confirm that it is possible to achieve high power factor operation with low harmonic distortion and satisfactory system performance under very low switching frequency conditions.

II. SELECTIVE HARMONIC ELIMINATION.

The power circuits in this paper consist of a Neutral Point Clamped-NPC converter working as active rectifier and a passive sinusoidal input filter. References [9]-[11] discuss the generalized method of Selective Harmonic Elimination and state that an arbitrary number M of harmonic can be controlled and/or eliminated from a standard three level output voltage waveform if it is chopped M times per half fundamental period. Expanding the waveform into Fourier series and assuming odd quarter-wave symmetry, the cosine components vanish and (1) gives n[th] harmonic coefficient of the sine components, (n = 1, 3, 5…).

$$a_n = (4E/\pi n)\sum_{k=1}^{M}(-1)^{k+1}\cdot\cos(n\alpha_k) \qquad (1)$$

$$0 \le \alpha_1 < \alpha_2 \cdots < \alpha_M < \pi/2$$

In order to control the fundamental component and eliminate (M-1) harmonics it is essential to solve a nonlinear and transcendental system of equations. Based on the algorithm in [9] it was developed a computer program to solve those equations intending to control the converter fundamental component and eliminate 5[th] and 7[th] harmonics.

III. SINUSOIDAL FILTER.

The sinusoidal input filter topology studied in this work takes up the classical concepts of harmonic filters from electric power systems together with a common solution for VSC active rectifiers [3]-[5]. Previous papers employed similar ideas in power electronics, but they recently reappeared under a high switching frequency modulation condition for a low power drive, [1].

The filter configuration in this work consists of a third order LCL filter plus some harmonic traps as in Fig. 1.

A. Minimum Reactive Power Optimized Filter Design.

Elementary filter theory recommends that the filter cut-off frequency f_{co} must be placed between the maximum desirable fundamental frequency f_1 and the first non-eliminated harmonic frequency f_D with separation factors between each one of them of at least 10. It results in a frequency separation equal to or greater than 100 between f_1 and f_D. This is difficult to achieve

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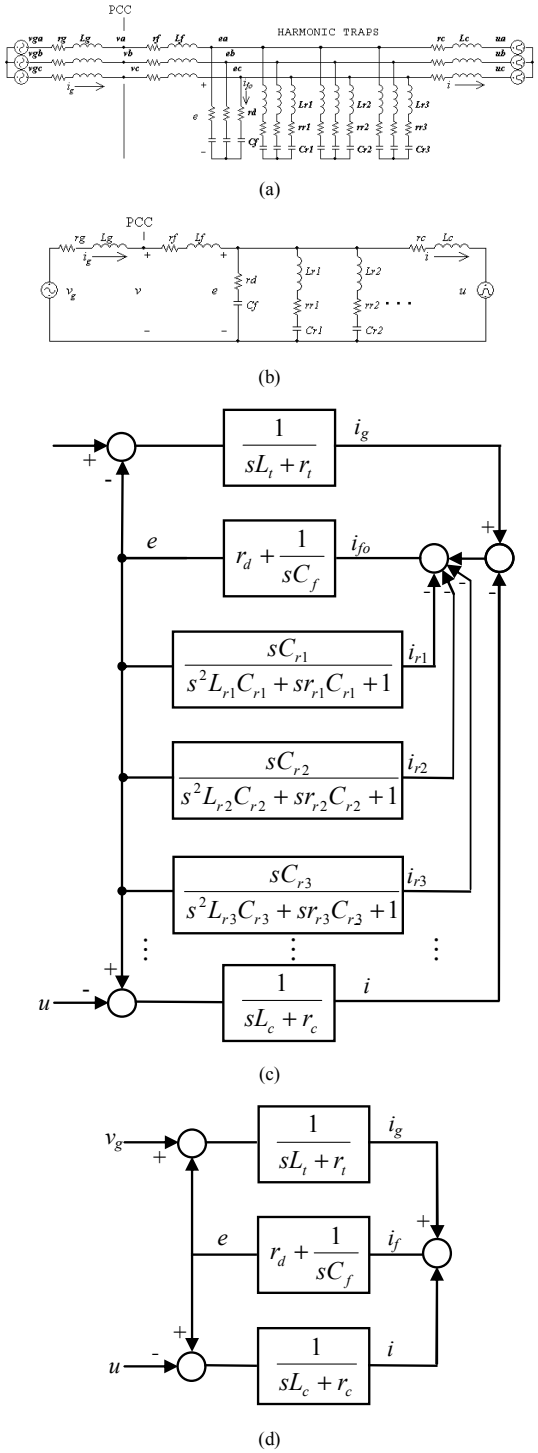


Fig. 1. Sinusoidal input filter and equivalent circuit.

with practically all modulation methods under low switching frequency conditions. For this reason, this work suggests a separation between f_1 and f_D of about 10 in the following way:

- The separation between f_1 and f_{co} must be greater than 5.
- The separation n_{scd} between f_{co} and f_D should be about 2.

Then it is possible to find out filter elements. The cut-off frequency can be generically expressed by:

$$f_{co} = 1/\sqrt{L_x C_y} \tag{2}$$

This expression leads to an infinite set of pair of values of L_x and C_y, which simultaneously suits this equation for a given value of f_{co} It requires new constraints to solve this problem. Various guidelines for filter design are presented in literature, [5]-[7] and [12], but they are either not feasible for low switching frequency applications or not enough restrictive to come up with a specific solution to the problem.

In [7] in order to limit the converter current ripple i_{rip} the converter side inductor L_c is given by:

$$L_c \le U_1 / 4\sqrt{6} f_c i_{rip} \tag{3}$$

At rated voltage, commutation frequency f_c = 180Hz and i_{rip} = 10% this results in L_c < 34%. Yet it provides a wide set possible element values. In [12], all filter inductors should be below 10%, which is not practical for many low switching frequency applications. Reference [6] restricts all filter inductors below 10% and imposes C_f = 5%, but the switching frequency is as high as 2.5 kHz. Reference [5] limits all inductors below 10% and C_f below 5%, but again the switching frequency is high, f_{sw} = 5-8 kHz.

The filter design optimization can be performed writing an algebraic expression for the total filter reactive power as a function of all reactive elements. This expression under the constraint of (2) represents the optimizing cost function by:

$$Q_{rt}(kVA_r) = f(L_1,...,L_i,C_1,...,C_j) \tag{4}$$

The first derivative of Q_{rt} equated to zero leads to the cost function critical points (maximums and minimums):

$$dQ_{rt}/dL_x = f'(L_1,...,L_i,C_1,...,C_j) = 0 \tag{5}$$

The second derivative of Q_{rt} leads to the cost function inflexions and concavity:

$$d^2Q_{rt}/dL_x^2 = f''(L_1,...,L_i,C_1,...,C_j) \tag{6}$$

The Fig. 2a shows behavior of the reactive power Q_{rt} versus the converter side inductor L_c. The critical points achieved with the above steps represent local maximum and minimum in the case of the filter proposed here. However neglecting the negative values of inductor L_c the Q_{rt} critical point can be regarded as global minimum as in Fig. 2b for different values of the parameter β_s, (which only depends on the filter design specifications: the voltage of C_f and the current of L_c and cut-off f_{co}). β_s is in general near to "1".

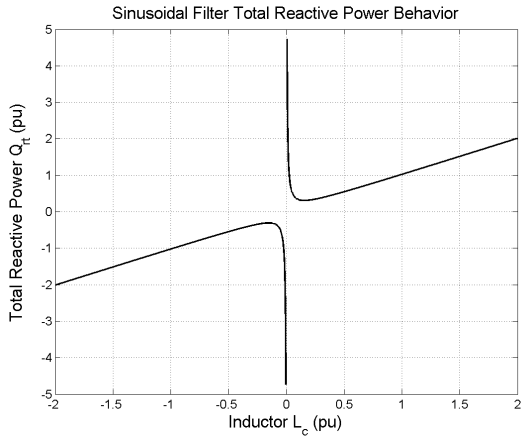
With this reasoning, it is possible to derive exact and simple closed form algebraic expressions for all filter reactive elements:

$$f_{co} = f_D / n_{scd} \tag{7}$$

$$L_c = \beta_s / f_{co} \tag{8}$$

$$C_f = 1/(\beta_s \cdot f_{co}) \tag{9}$$

Yet, the filter design must assure a resonant frequency f_{res} below the lower harmonic set resultant from the modulation process. Because of its superior output harmonic spectrum SHEPWM makes the choice of f_{res}



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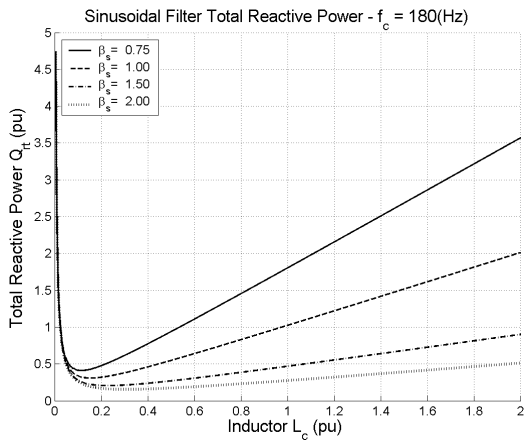


(b)

Fig. 2. Total Reactive power behavior as function of the converter side inductor and the parameter β_s.

easier than other classical modulator, [8] and [11]. This work suggests the expression for f_{res}:

$$f_{res} = \left[f_D + \text{ceil}(f_{co})\right]/2, \quad (10)$$

which intuitively allocates f_{res} between f_{co} and f_D. Then:

$$L_{eq} = \beta_s^2 / \left(f_{res}^2 \cdot L_c\right) \quad (11)$$

$$L_f = \left[\left(L_c \cdot L_{eq}\right) / \left(L_c - L_{eq}\right)\right] - L_g \quad (12)$$

Fig. 3 represents a summary of the *MRP-OFD* and produces the element values presented in Table I and II. It is remarkable that the *MRP-OFD* results in all main filter elements about 15% with f_c = 180Hz and f_c = 420Hz.

Filter damping is another important designing aspect. Again, the literature presents various different recommendations, [1], [3], [5], [13]-[17]. In [13] the filter is over damped. Reference [14] designs its filter with critical damping. In contrast to them, [1] shows that under damped filters present better attenuation. Following this line [5] adopts filter quality factors Q = 1.8 and 3.6, and [3] chooses Q = 7.7. Additionally [15]-[17] discusses many alternative for resistive damping process, but according to [17] the better one consists in placing the damping resistor in series with capacitor C_f. It is recognizable that passive damping has many collateral effects over the filter. One of them is deterioration in

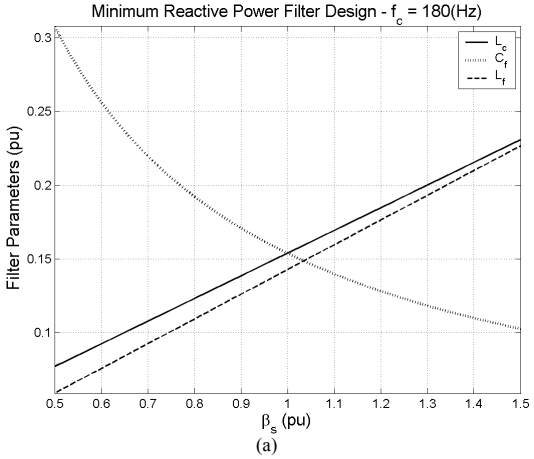
TABLE I
MINIMUM REACTIVE POWER OPTIMIZED FILTER DESIGN.

f_c	f_D	f_{co}	f_{res}
180Hz	660Hz	390Hz	540Hz
3.0pu	11.0pu	6.5pu	9.0pu
420Hz	1380Hz	815Hz	1110Hz
7.0pu	23.0pu	13.6pu	18.5pu

TABLE II
RATINGS OF SINUSOIDAL FILTER ELEMENTS.
(U_{base} = 4160V, S_{base} = 5MVA, β_S = 1).

f_c (Hz)	L_c	L_f	C_f
180Hz	1.4123mH	1.3103mH	117.92µF
	0.15385pu	0.14274pu	0.15385pu
420Hz	0.67543mH	0.56245 mH	56.398µF
	0.07358pu	0.06127pu	0.07358pu

L_g = 0,025 pu, L_g = 0,22949 mH.



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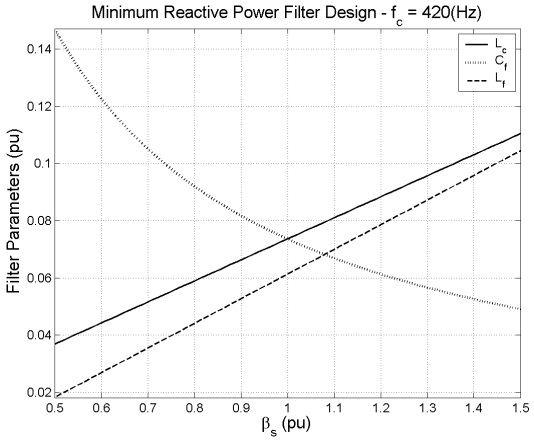


(b)

Fig. 3. Optimized filter design, a) f_c = 180Hz and b) f_c = 420Hz.

filter attenuation. This is reasonably compensated by the addition of series resonant harmonic traps in parallel to the shunt branch of C_f. The number of resonant traps depends on the desired system specification and they should be tuned in the first non-eliminated harmonic frequencies. Each branch has to be designed individually with the *MRP-OFD* to achieve minimum total filter reactive power. They also must be very selective, (Q > 10). Reduction in system efficiency is another trouble of

passive damping. However if there is enough control bandwidth active damping can solve the two difficulty presented. On the contrary, this paper suggests a hybrid solution involving both passive and active damping.

B. Filter Evaluation.

After the optimized design, it is possible to evaluate the filter performance. Fig. 4 and 5 bring its frequency response for the grid current i_g and voltage v, at point common coupling PCC, in relation to converter voltage u. These figures show that damping deteriorates the filter attenuation (from expected -60dB/dec to about -40 dB/dec) though it is effective in reducing the risk of filter resonance.

The dynamic stiffness allows evaluating filter disturbance rejection capacity. Fig. 6 and 7 exhibit this feature with the *MRP-OFD* for the grid voltage with respect to the current and voltage at PCC. These figures point up that the filter dynamic stiffness is better in the high frequency region. It reflects the filter sensitivity to disturbances near the fundamental frequency, which is important to avoid. Nevertheless, it has more to do with the third order filter configuration, (whose disturbance rejection capacity is poor [17]), rather than with the proposed design procedure.

The filter installed between the utility grid and the converter also increases the power demands that converter must be able to deal with. It increases the converter voltage and current ratings. It is possible to show that it depends only on the filter configuration and size of its elements. Equations (13) and (14) respectively describe the converter voltage and current at fundamental frequency of an active rectifier.

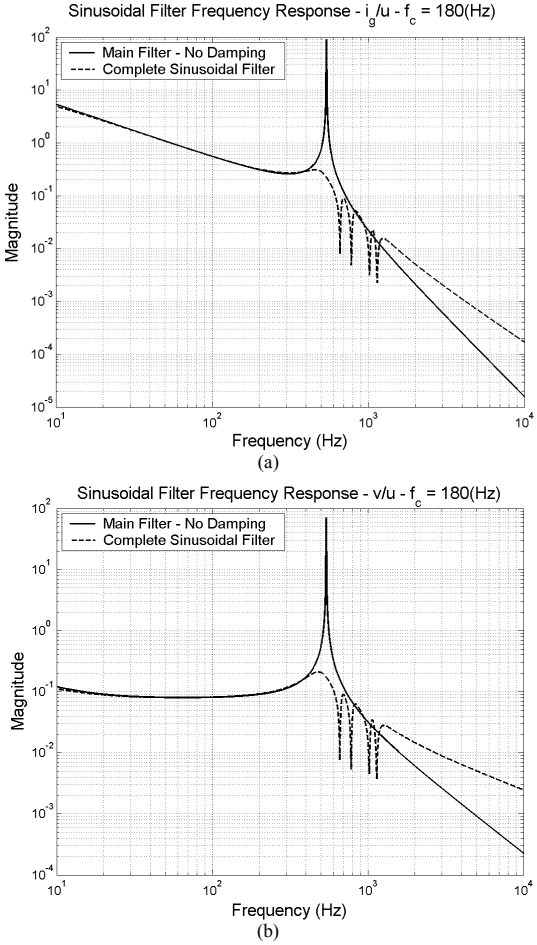


Fig. 4. Sinusoidal filter frequency response, a) i_g/u and b) v/u

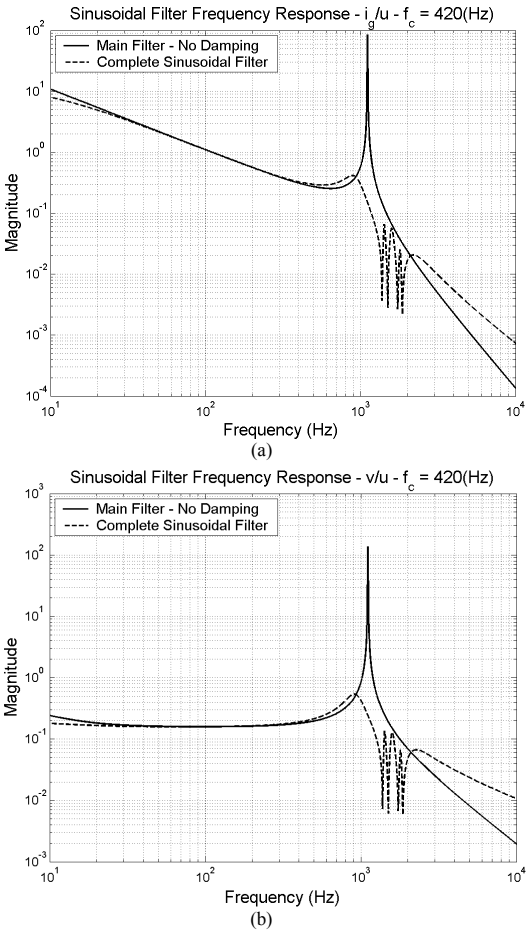


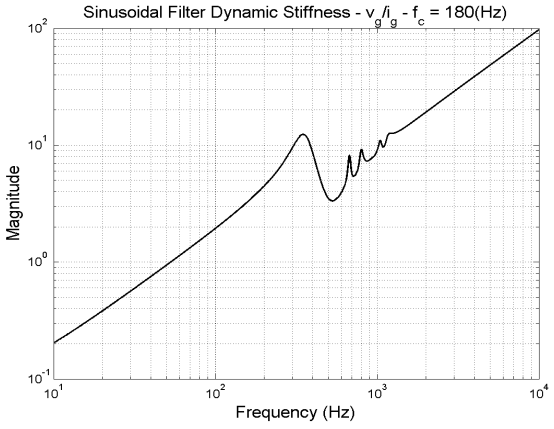
Fig. 5. Sinusoidal filter frequency response, a) i_g/u and b) v/u.

$$u = H_i(j\omega_1)v - \left[\left(r_c + j\omega_1 L_c\right) + \left(r_f + j\omega_1 L_f\right)H_i(j\omega_1)\right]\cdot i_g \quad (13)$$

$$i = -\left[\frac{j\omega_1 C_f}{\left(1 + j\omega_1 r_d C_f\right)}\right]v + \left[1 + \frac{\left(r_f + j\omega_1 L_f\right)\cdot j\omega_1 C_f}{\left(1 + j\omega_1 r_d C_f\right)}\right]i_g \quad (14)$$

$$H_i(j\omega_1) = 1 + \left[\left(r_c + j\omega_1 L_c\right)\cdot\left(j\omega_1 C_f\right)/\left(1 + j\omega_1 r_d C_f\right)\right] \quad (15)$$

There are absolute and relative increments in these two converter ratings, Δu_a, Δi_a and Δu_r, Δi_r respectively (16)-(19). The former is associated with voltage drop in the series elements and current drawn in shunt branches. The latter is an extension of the concepts of voltage and current regulation in electrical system. Table III shows those increments with the *MRP-OFD* at rated voltage and current. The table shows that the absolute increments are always positive and greater than the relative ones. The increments Δi_r are negative confirming the expectation that the filter will not require a converter over sizing. It means that converter current demand is smaller with the



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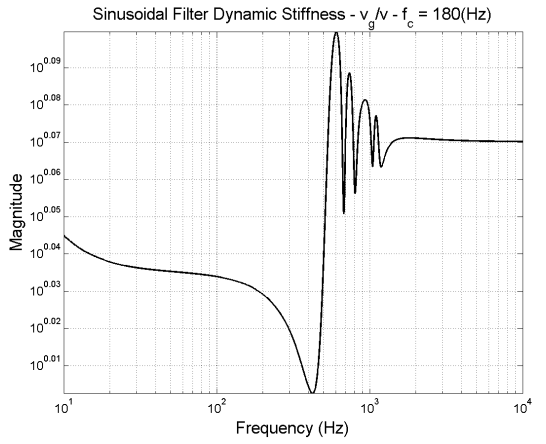

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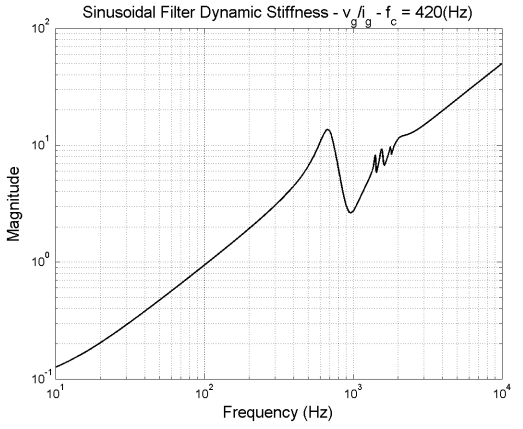
Fig. 6. Sinusoidal filter dynamic stiffness a) v_g/i_g and b) v_g/v.



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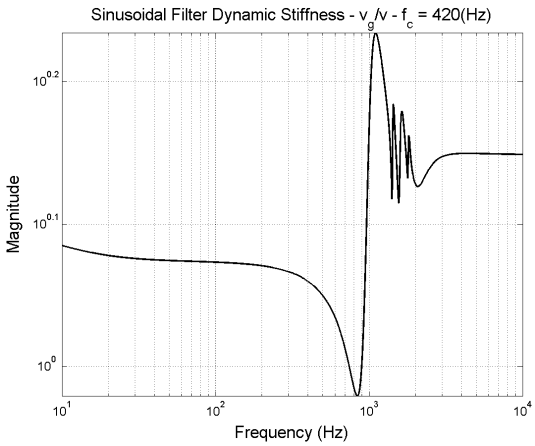


(b)

Fig. 7. Sinusoidal filter dynamic stiffness a) v_g/i_g and b) v_g/v.

filter than without it due to both the capacitive effects and the *MRP-OFD*. In addition, the converter tolerates the increment of 0.16% in its voltage after the filter installation. Here it is important to emphasize that is the relative increments in those quantities, rather than the absolute ones that must be considered for a converter design since it is more realistic, [7].

$$\Delta u_a = \left[H_i(j\omega_1)-1\right]v - \left[\left(r_c + j\omega_1 L_c\right) + \left(r_f + j\omega_1 L_f\right)H_i(j\omega_1)\right]\cdot i_g \quad (16)$$

$$\Delta i_a = \frac{\left[\left(r_f + j\omega_1 L_f\right)\cdot i_g - v\right]\cdot j\omega_1 C_f}{\left(1 + j\omega_1 r_d C_f\right)} \quad (17)$$

$$\Delta u_r = |u| - |v| \quad (18)$$

$$\Delta i_r = |i| - |i_g| \quad (19)$$

IV. Voltage Oriented Current Control.

A classical voltage oriented synchronous reference frame current loop controls a three-level NPC rectifier. In this case, the current components i_d and i_q controls dc bus voltage and reactive power respectively and produce the reference voltage commands u_d and u_q which are transformed from *dq* to *abc* and them applied to the modulator.

V. Results.

A three-level NPC rectifier of 5MVA/4160V 60Hz with dc bus voltage v_{dc} = 3236V and switching command generated by SHEPWM at the commutation frequency f_c = 180Hz is simulated with MATLAB6.5/SIMULINK. The sinusoidal filter elements are all about 0.15pu (Table IV). The system short-circuits inductance L_g is assumed equal to 0.025 pu. The rectifier is under control of voltage oriented synchronous reference frame current loop and the converter high power factor is achieved by setting the reference current i_q =-148 A by a control action.

TABLE III
Voltage and Current Demands after Filter Installation.

f_c (Hz)	Δu_a (%)	Δu_r (%)	Δi_a (%)	Δi_r (%)
180	29.427	0.16319	15.2670	-2.01070
420	13.642	-1.5651	7.2457	-0,41910

TABLE IV
Voltage and Current Demands after Filter Installation.

f_c (Hz)	L_c	L_f	C_f
180Hz	1.375mH	1.272mH	120μF
	0.1498 pu	0.1385 pu	0.1566 pu

L_g = 0,025 pu, L_g = 0,22949 mH.

In Fig. 8a, U_{ab} exhibits a typical 3-level Line voltage standard along with a grid voltage V_{ab} nearly sinusoidal. In this case the former presents a *THD* = 26.61% and negligible low frequency harmonics below 660Hz and the latter presents a *THD* = 0.4% with very low harmonic content in all frequency range, (as in Fig. 9a). In Fig. 8b V_a and i_a are basically in phase. The displacement power factor $DPF \approx 1$ and distortion factor given by $DF = (I_{s1}/I_s) = 1/[(THD)^2+1]^{1/2} \approx 1$ in [18]. It results in system operation essentially with unity power factor ($PF = DPF.DF$). Moreover i_a is highly sinusoidal with *THD* = 1.37% and all current harmonic amplitudes below 0.8%, (Fig. 9b). In contrast, when the filter is removed the harmonic distribution and distortion deteriorate, as one would expect. In Fig. 10, the grid voltage and current at the PCC become distorted and their *THD* in Fig. 11 increase to 3.77% and 11.93% respectively. The converter *THD* = 26.04% is practically constant.

Fig. 11 and 12 illustrate the system performance under

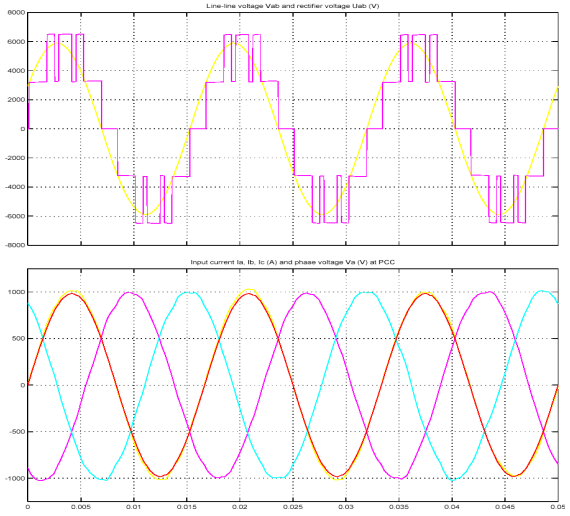


Fig. 8. a) Line grid V_{ab} and converter U_{ab} voltages b) grid currents i_a, i_b, i_c and phase voltage V_a (in red) with sinusoidal filter.

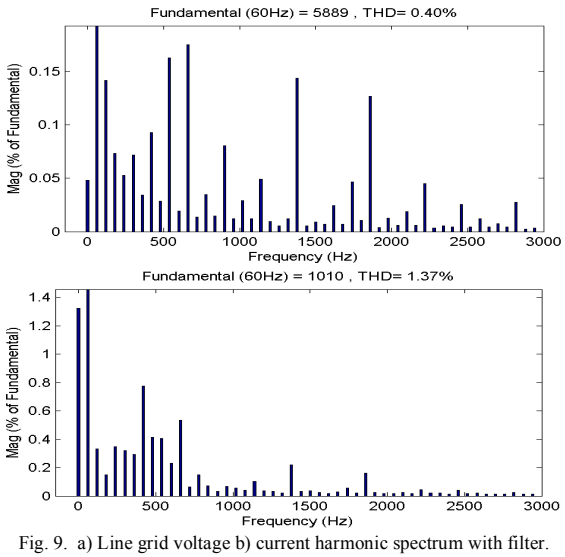


Fig. 9. a) Line grid voltage b) current harmonic spectrum with filter.

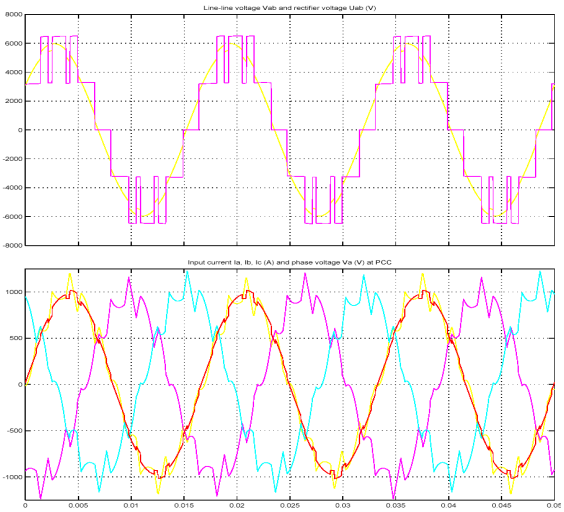


Fig. 10. a) Line grid V_{ab} and converter U_{ab} voltages b) grid currents i_a, i_b, i_c and phase voltage V_a (in red) without sinusoidal filter.

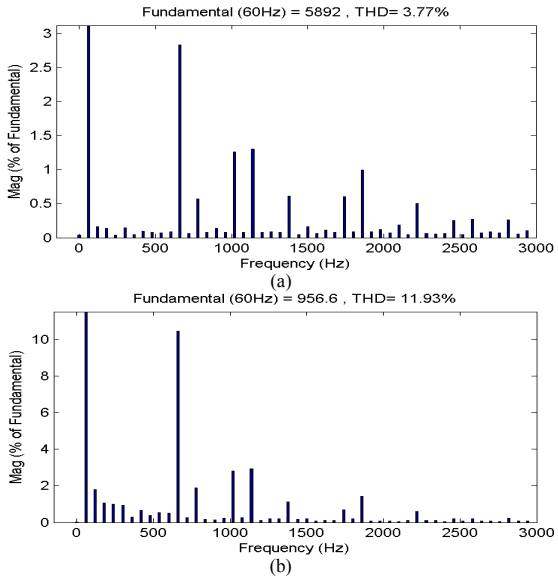


Fig. 11. a) Line grid voltage b) current spectrum without filter.

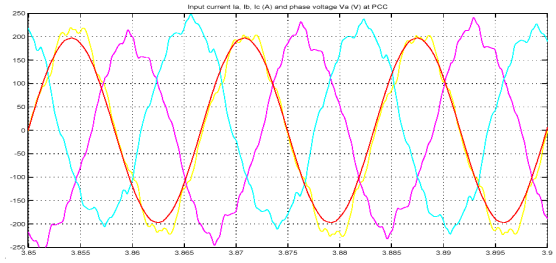
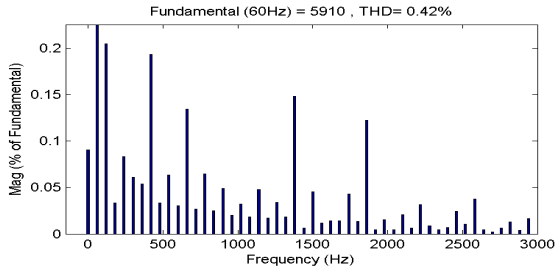


Fig. 12. Grid currents i_a, i_b, i_c and phase voltage V_a (in red) with sinusoidal filter and reduced grid current (to 0.2 pu).

light load. Following an increase in dc load to 5 pu, the grid current reduces to 0.2 pu. In this case again the V_{ab} is almost sinusoidal and its *THD* = 0.42% is very close to that under full-load condition. On the other hand, although the current i_a seems to be less sinusoidal their *THD* = 7.79% is lower than 11.93% (full-load condition



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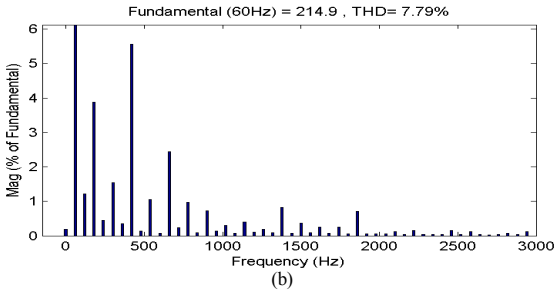

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Fig. 13. a) Line grid voltage V_{ab} b) current i_a, harmonic spectrum with filter and reduced load.

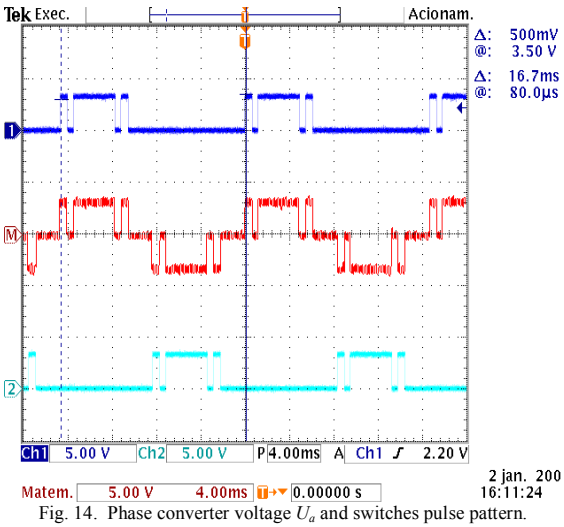

Fig. 14. Phase converter voltage U_a and switches pulse pattern.

without filter). The reduced current condition shows that system performance is also satisfactory ($DPF \approx 0.98$ and $DF \approx 1.0$) resulting in a high power factor operation even under reduced load and switching frequency conditions.

Experimental results from a lab test bench for SHEPWM with Texas DSP TMS320F2812 are in Fig. 14-16. Fig. 14 and 15 shows the converter pulse pattern a long with the phase and line voltage shapes. The line voltage spectrum in this case is in Fig. 16. The Table V shows the voltage amplitude of the first 20 odd line harmonic voltages.

VI. CONCLUSIONS

This paper presented an enhanced passive filter configuration for a high power converter. It also discussed a complete filter design, performed at a point of minimum reactive power. Besides, a reasonably simple

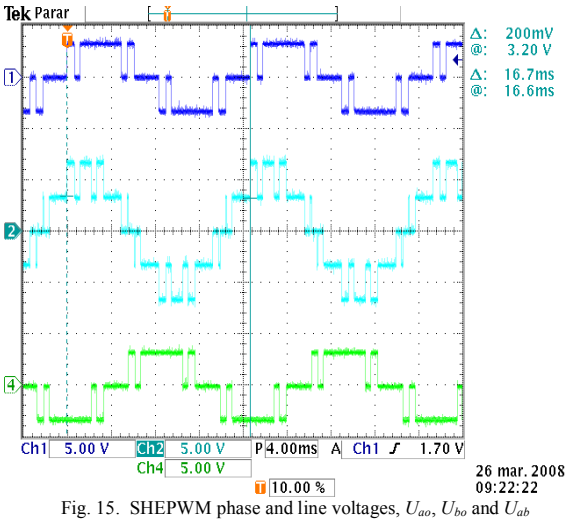

Fig. 15. SHEPWM phase and line voltages, U_{ao}, U_{bo} and U_{ab}

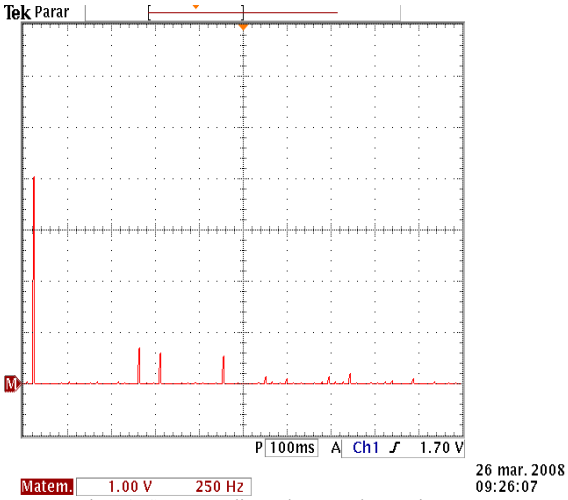

Fig. 16. SHEPWM line voltage U_{ab} harmonic spectrum.

TABLE V
SHEPWM-LINE VOLTAGE HARMONICS.

N	*Frequency* f_n (Hz)	U_n (%)
1º	60	100.00000
3º	180	0.93443
5º	300	1.43095
7º	420	0.56376
9º	540	0.25467
11º	660	17.17404
13º	780	14.85169
15º	900	1.03137
17º	1020	0.63141
19º	1140	14.75186

and intuitive procedure culminates in few design steps. *MRP-OFD* permits to derive closed form expressions for the filter element, which specifies unique and well-defined element values. *MRP-OFD* states a minimum filter elements for a given design specification and since it is generically developed, it can be easily employed in adjustable speed drive filter design. After the optimized design, the paper presented an evaluation of the filter performance. The filter frequency response showed that damping deteriorates filter attenuation though it was

effective in reducing the risk of filter resonance. The addition of harmonic traps in parallel to the shunt branch compensates around the fundamental frequency this loss of attenuation in high frequency region. Besides, this evaluation showed that the filter dynamic stiffness is poor. However it is influenced by the main filter (third order LCL) configuration rather than the proposed design procedure. The paper showed as well that due to capacitive effects and an adequate filter design the converter could tolerate the variations of voltage and current after the filter installation without overrating. The modulation strategy in this paper was the Selective Harmonic Elimination-SHEPWM. The modulator eliminates harmonics up to the 11^{th}. It creates sufficient frequency separation to set cutoff and/or resonance frequencies and simplifies the filter design rules. Furthermore, the modulator SHEPWM worked in a classical voltage oriented synchronous reference frame control of a high power active rectifier. Simulation and experimental results confirmed that it is possible to achieve controllable displacement power factor with low input harmonic distortion and reduced filter kVAr rating with very low switching frequency and, in both full and reduced load conditions.

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